

U.S. Department of Commerce, Patent and Trademark Office					Atty Docket No.		Serial No.	
					SP-2617 US		09/411,469	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT					Applicant(s)			
(Use several sheets if necessary)					Banerjee, Chandramouli; Tremblay, Marc			
Filing Date					Group			
October 1, 1999					2787			

U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,574,939	Nov. 12, 1996	Keckler et al.	395	800	
	AB	5,657,291	Aug. 12, 1997	Podlesny et al.	365	230.05	
	AC	5,721,868	Feb. 24, 1998	Yung et al.	395	476	
	AD	5,742,782	Apr. 21, 1998	Ito et al.	395	386	
	AE	5,761,475	Jun. 2, 1998	Yung et al.	395	394	
	AF	5,764,943	Jun. 9, 1998	Wechsler	395	394	
	AG	5,778,248	Jul. 7, 1998	Leung	395	800.23	
	AH						
	AI						
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	AK						

Foreign Patent Documents							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AL	0395348A	Oct. 31, 1990	EP				
	AM	0672681A1	Dec. 7, 1994	EP				
	AN							
	AO							
	AP							

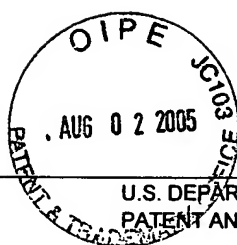
  

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)		
AQ	Piepho, R.S., et al; "A Comparison of RISC Architectures" <u>IEEE Micro</u> , IEEE Inc., New York, U.S. Volume 9, No. 4, August 1, 1989, Pages 51-62.	
AR	"Multiple Queued Condition Codes" <u>IBM Technical Disclosure Bulletin</u> , IBM Corp., New York, U.S., Volume 31, No. 2, July 1998, Pages 294-296.	
AS	M. Fillo et al.: "The M-Machine Multicomputer;" Proceedings of the Annual International Symposium on Microarchitecture, U.S., Los Alamitos, IEEE Comp. Soc. Press, Vol. SYMP. 28, 1995, pages 146-156, XP000585356 ISBN: 0-8186-7349-4	

Examiner	Date Considered
<p>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.</p>	

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	AQ	M. Berekovic et al.: "Hardware Realization of a Java Virtual Machine For High Performance Multimedia Applications;" 1997 IEEE Workshop on Signal Processing Systems. SIPS 97 Design and Implementation Formerly VLSI Signal Processing, pages 479-488, XP002139288, 1997, New York, NY, USA, IEEE,						
	AR	S. W. Keckler et al.: "Processor Coupling: Integrating Compile Time and Runtime Scheduling for Parallelism;" Proceedings of the Annual International Symposium on Computer Architecture, U.S., New York, IEEE, Vol. SYMP. 19, 1992, pages 202-13, XP000325804 ISBN: 0-89791-510-6						
	AS							
Examiner			Date Considered					
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FORM PTO-892	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	SERIAL NO. 09/411,469	GROUP ART UNIT 2124	ATTACHMENT TO PAPER NO. 6
NOTICE OF REFERENCES CITED		APPLICANT(S) Tremblay et al.		

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*		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	A	6,263,424	7/2001	Tran et al.	712	221	
	B	4,893,267	1/1990	Alsup et al.	708	518	
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*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS
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EXAMINER Chuong D. Ngo	DATE June 12, 2002	Form892ccs2106b
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\* A copy of this reference is not being furnished with this office action.  
(See Manual of Patent Examining Procedure, section 707.05(a).)